Digital Front End Crate Controller

Printed Circuit Board Fabrication

Jamieson Olsen 3 May 2000

General Information

board revision: A

board size: 233.25mm x 320mm board thickness: 0.093" +/- 10%

board material: FR4 layers: 6 controlled impedance: No

copper: ½ oz TOP and BOTTOM, 1oz all other layers

solder mask: BOTH sides, LPI, Black silk screen: BOTH sides, White traces: 7 mil line / 7 mil space "White Tin" plating

Filenames

All gerbers are POSITIVE IMAGE. Gerber files are in RS254-X format.

TOP routing layer GROUND plane TOP INNER routing layer 3V power plane 5V power plane BOTTOM routing layer	<pre>dfec_top.gbr dfec_gnd.gbr dfec_inr.gbr dfec_v3 .gbr dfec_v5 .gbr dfec_bot.gbr</pre>
soldermask top soldermask bottom silkscreen top silkscreen bottom	<pre>dfec_smt.gbr dfec_smb.gbr dfec_sst.gbr dfec_ssb.gbr</pre>
drill tape #1 drill tape #2	thruhole.tap 2_7.tap
fabrication drawing	dfec_drd.gbr
assembly drawing top assembly drawing bottom	<pre>dfec_ast.gbr dfec_asb.gbr</pre>

Layer Stackup

This board does not require controlled impediances. Note: total board thickness should be 0.093" +/- 10%. Follow the layer order shown below.

1. TOP ROUTING LAYER ("COMPONENT" SIDE)

CORE

2. PLANE LAYER

PRE-PREG

3. INNER ROUTING LAYER

CORE

4. VCC3 POWER PLANE

PRE-PREG

5. VCC5 POWER PLANE

CORE

6. BOTTOM ROUTING LAYER ("SOLDER" SIDE)

Colors

soldermask: LPI BLACKsilkscreen: WHITE

Thruholes

- 10 different hole sizes, some of which are NON-PLATED.
- 813 holes total
- 0.381mm hole is smallest
- 3.000mm hole is largest
- no blind or buried vias
- refer to dfec_drd.gbr for fabrication data and hole legend

Contact Prints

The fabricator shall generate photoplots and sent them to Fermilab for approval prior to fabrication.

Board Testing

Bare boards must be tested with either a flying head probe or a bed of nails fixture. Each tested good board must be clearly stamped or marked with paint.

Mechanical Considerations

The overall board dimensions are 233.25mm x 320mm. The TOP and BOTTOM edges of the board must be beveled or milled as specified in the dfec_ast.gbr drawing.

Contact Information

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